Reg. No. : 9 2 0 2 2 3 1 0 4 0 1 4

Question Paper Code : 40917

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2024.

Third Semester

Computer Science and Engineering

CS 3351 — DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

(Common to : Computer Science and Design/Computer Science and Engineering (Artificial Intelligence and Machine Learning)/Computer Science and Engineering (Cyber Security)/Computer and Communication Engineering/Artificial Intelligence and Data Science/Computer Science and Business Systems/Information Technology)

(Regulations 2021)

(Also common to PTCS 3351 – Digital Principles and Computer Organization for – Regulations 2023)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Write down the difference and borrow expressions of full subtractor.
2. How many selection inputs, data inputs and outputs for 1×32 DEMUX?
3. Compare latch and flip flop.
4. How many flip flops are required for designing mod 17 counter? Justify.
5. What is the role of control unit in the operation of digital computer?
6. Differentiate assembly level language and high level language.
7. What is pipelining?
8. Mention the two approaches used for generating control signals.
9. What is the purpose of cache memory?
10. What is virtual memory?

PART B — (5 × 13 = 65 marks)

11. (a) With neat diagram, explain the working of 4-bit binary adder-subtractor. (13)

Or

(b) Explain the working of four – input priority encoder with its truth table and block diagram. (13)

12. (a) Describe S-R and T flip flops with the help of block diagrams and characteristic tables. (13)

Or

(b) Explain the working of 4-bit shift left and shift right registers using D flip flop. (13)

13. (a) Explain the functional units of digital computer with block diagram. (13)

Or

(b) Explain about any four addressing modes with example. (13)

14. (a) Describe micro programmed control unit. (13)

Or

(b) Describe control hazards. Explain with suitable techniques, how control hazards can be avoided. (13)

15. (a) Explain the working principle of DMA with neat diagram. (13)

Or

(b) Explain the architecture of USB. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Design 8 × 1 MUX. Implement the boolean function F (A, B, C, D) = Σ (1, 3, 4, 11, 12, 13, 14, 15) using 8 × 1 MUX. (15)

Or

(b) Design Mod-5 Synchronous counter using J – K flip flop. (15)

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